State-of-the-Art Ion-Implanted Low-Noise GaAs MESFET's and High-Performance Monolithic Amplifiers

KEMS-GWOR WANG, MEMBER, IEEE, AND SHING-KUO WANG, MEMBER, IEEE

Abstract—**State-of-the-art GaAs low-noise MESFET's and high-performance monolithic amplifiers have been fabricated using a high-yield, planar ion-implantation process. A 0.5-μm-gate FET has achieved a 1.2-dB noise figure with 8.8 dB associated gain at 12 GHz and a 1.7-dB noise figure with 6.6 dB associated gain at 18 GHz. A 0.25×60 μm FET has achieved 1.7 dB and 2.5 dB noise figures with 6.3 dB and 5.0 dB associated gains at 22 GHz and 35 GHz, respectively.**

A two-stage monolithic amplifier using the 0.5-μm FET process has achieved a 1.8-dB noise figure with 23.6 dB associated gain at 9.5 GHz. The dc yield of the amplifier chips is better than 40 percent.

These results have demonstrated that direct ion implantation is capable of producing low-cost, high-performance low-noise monolithic microwave integrated circuits (MMIC's).

I. Introduction

THE MAIN OBJECTIVE of this work is to develop a high-performance, production-adaptable FET process for low-noise MMIC applications. Due to its low cost, good uniformity/reproducibility, high throughput, and capability of selective doping, ion implantation is the preferred technique of active layer formation for high-volume GaAs MMIC production [1]–[3]. However, the best reported GaAs low-noise MESFET performance had been obtained from either epitaxial materials or ion implantation into buffer layers [4]–[10].

This paper reports the state-of-the-art performance of the GaAs low-noise FET's fabricated using a planar, direct ion-implantation process. Key features of this process include a shallow, highly doped channel layer, selective N^+ contact layers, and planar isolation by proton bombardment. A two-stage *X*-band monolithic low-noise amplifier using this FET process has also demonstrated state-of-the-art noise performance comparable to the results reported by Lehman and Heston [11].

II. Noise Considerations

Submicron gate length is essential for high gain and low noise in GaAs microwave/millimeter-wave devices. In these short-gate devices, electrons reach saturation velocity under the gate. The high field diffusion noise [12]–[14], which is linearly dependent on the drain current, dominates in this velocity-saturated channel region. Fortunately, there is a strong correlation between the drain noise and the induced gate noise, which leads to a high degree of cancellation in the overall noise output of the GaAs FET. Pucel *et al.* suggested that a larger noise cancellation could be achieved by using a thin channel layer [13], [14]. The large gate-length-to-channel-thickness ratio confines the electric field in the horizontal direction, resulting in better control of electron flow by the gate potential and sharp pinch-off. By using a thin active layer, one can also suppress the increase of hot-electron noise temperature at the drain end of the channel by reducing the high field distribution in that region [15]. From their derivation, Cappy *et al.* [16] had found that the FET noise K_f factor (a proportionality factor in Fukui's noise equation [17]) can be reduced by decreasing the active layer thickness. As they asserted, this is the main reason for the noise superiority of HEMT over MESFET due to the very thin two-dimensional electron gas (2 DEG) layer involved.

Although, as pointed out above, the device intrinsic noises can be minimized by using a thin active layer, negative effects can result from extrinsic parasitic resistances. High source resistance associated with the small channel cross section greatly degrades the device noise/gain performance. The parasitic resistance not only contributes to the thermal noise, but also prevents the full cancellation of the correlated drain and gate noises in the intrinsic transistor [12]. Moreover, poor device pinch-off (high output conductance) always occurs in these short-gate, thin-channel devices [6], [7], [9], [10]. Those extrinsic parasitic resistances and the short-channel effect must be minimized in order to achieve the best low-noise performance. Daembkes *et al.* [18] pointed out that those effects can be alleviated by highly doping the channel layer. However, their 0.4-μm-gate device results did not meet expectations, probably due to a nonoptimized process.

The above considerations prompt us to use a shallow, high-dose, ion-implanted channel layer for an optimized low-noise FET. An additional advantage of the low-energy implant is an abrupt doping profile at the channel–

Manuscript received May 1, 1987; revised July 13, 1987.

The authors are with the Torrance Research Center, Hughes Aircraft Company, Torrance, CA 90509.

IEEE Log Number 8717250.

0018-9480/87/1200-1501$01.00 ©1987 IEEE

TABLE I
SUMMARY OF NOISE-REDUCTION APPROACHES IN THIS WORK

	Minimize Intrinsic Noises	Minimize Parasitic Resistance & Capacitance	Maintain High Transconductance Near Pinch-Off	Reduce Short Channel Effect	Reduce Schottky Gate Leakage Current
0.25 to 0.5 μm Gate Length	√		√		
Shallow, Abrupt Channel Layer by Low Energy Implant (70 KeV)	√		√	√	
High Channel Doping (5×10^{17}cm^{-3})	√	√	√	√	
Source Drain N^+ Contact Layers (1×10^{18}cm^{-3})		√	√		√
Gate Offset Toward Source Contact		√	√		
Low Current Density (140 mA/mm)	√				√
Proton Implant Isolation Under Gate Pads		√			

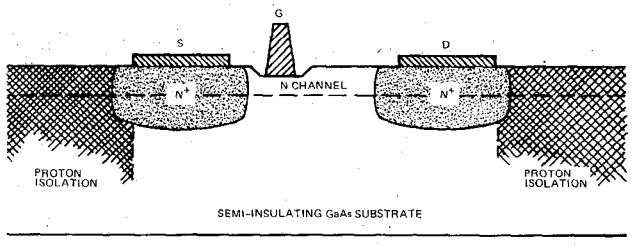

Fig. 1. Structure of the optimized low-noise GaAs MESFET made by ion implantation. Shallow, high-dose single implant is used for the active channel layer. Additional double implants are done under the source and drain contacts. High-dose proton bombardment is used for device isolation.

substrate interface, from which the FET can maintain high transconductance (g_m) and high mobility near the pinch-off region. Thus, the best device noise performance can be obtained at a very low drain bias current, where the high field diffusion noise is correspondingly low and the device minimum noise figure is not increased due to g_m degradation [13], [19].

In this work, we are able to maximize the FET transconductance near pinch-off by using a 70-keV Si implant to form a heavily doped thin channel layer, and at the same time minimize the source resistance by using selective implants to form N^+ layers under the source and drain contacts. Proton bombardment is used to reduce the parasitic capacitance between gate and source pads, which is detrimental to the device cutoff frequency [20]. Table I summarizes our approaches for noise reduction in this work. The cross section of the device structure is illustrated in Fig. 1.

III. FABRICATION OF LOW-NOISE FET'S

The devices reported here use Hughes's standard 0.5 × 300 μm low-noise PI-300 FET geometry, as shown in Fig. 2. The source–drain spacing is 3 μm. Device fabrication starts with the channel layer formation by direct implantation of $^{28}Si^+$ ions into a semi-insulating GaAs substrate

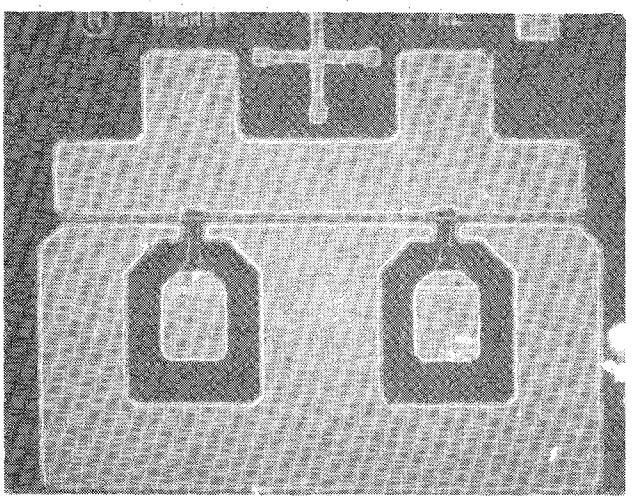

Fig. 2. Layout of the 0.5×300 μm low-noise FET. The source–drain spacing is 3 μm and the unit gate width is 75 μm with two gate feeds.

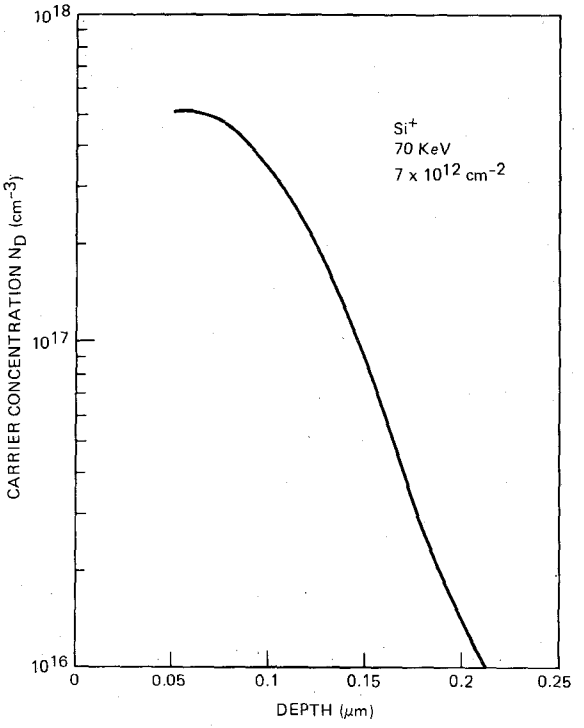

Fig. 3. The measured carrier concentration profile with a 70-keV and 7×10^{12} cm^{-2} Si^+ direct ion implantation into a LEC GaAs semi-insulating substrate. Profile was obtained by successive etching and capacitance–voltage measurements.

wafer with 70 keV energy and 7×10^{12} cm^{-2} dose. Next, N^+ contact layers are selectively implanted into the source/drain contact regions to minimize the source resistance. We use 130-keV, 2×10^{13} cm^{-2} and 50-keV, 8×10^{12} cm^{-2} double Si implants to create an N^+ doping of about 1×10^{18} cm^{-3} to a depth of about 0.15 μm. These implants are activated by capless annealing at 850°C for 30 min under As_4 overpressure. The free-carrier concentration of the channel layer obtained by successive etch removal and C–V measurement is shown in Fig. 3. The peak carrier concentration is about 5.1×10^{17} cm^{-3} at 550 Å depth

from the surface with an effective channel thickness of about 1200 Å. Doping sharpness is less than 650 Å from $1\times10^{17}\,cm^{-3}$ to $1\times10^{16}\,cm^{-3}$ of carrier concentration.

The FET source/drain ohmic electrodes are formed using AuGe/Ni/Au metal and alloyed at 380°C for 60 s. This temperature cycle is found to yield the best contact resistance without degradation of surface morphology. Smooth ohmic contact edges and surface are important for preventing current crowding and achieving high yield for submicrometer gates. Contact resistance of less than 0.1 $\Omega\cdot$mm is routinely achieved. This process produces FET's with an average saturation current of 160 mA/300 μm and a standard deviation of 3.6 percent across a 2-in wafer.

Device isolation is achieved by proton bombardment with 100 keV energy and $2\times10^{14}\,cm^{-2}$ dose to minimize the pad capacitance and result in a planar surface. This high degree of isolation is important for minimizing the circuit RF loss in MMIC fabrication. The isolation current is usually less than 5 μA at 200 V bias between two active layers which are 100 μm apart.

This planar process, along with smooth ohmic surface, allows intimate mask contact to the wafer in the contact photolithography process, which is critical to achieving high yield for the 0.5-μm gate fabrication. The nominal gate length is 0.5 to 0.55 μm. Because of the shallow channel layer, very shallow gate recess etch (about 400 Å) is required before the Ti–Al gate metallization and lift-off. The shallow gate recess etch leads to small variation of device parameters. Next, a Ti–Au overlay metal is formed for low-resistance bonding. Fabrication is completed by a precision lapping and backside metallization. After scribe and break, each device is dc tested and wire bonded in a 50-Ω fixture for RF testing.

IV. Low-Noise FET's Performance

Of the 250 chips tested, 118 passed the visual test and the dc specification, for a 47 percent dc yield. Visual rejects include open or dented gate, stain or contamination, cracked or chipped chip, and unwanted or missing gold. The dc specifications for passage include I_{dss} of 38 to 46 mA and V_{po} of 1.2 to 1.6 V. Fig. 4 shows a typical $I-V$ characteristic of the 0.5-μm low-noise FET. The device shows good saturation behavior (low output conductance) and sharp pinch-off. Fig. 5 shows the transconductance as a function of gate bias for the low-noise FET. High transconductance, about 100 mS/mm, is achieved near pinch-off, which indicates a sharp channel–substrate interface resulted from the highly doped, shallow channel layer. The device also shows a high-quality Schottky gate. The barrier height is determined to be 0.7 V with an ideality factor of less than 1.2 and a gate/source breakdown voltage as high as 35 V, as seen in Fig. 6. This is believed to be the result of the low channel current and the shallow, highly doped channel layer. The uniformity is good. Fig. 7(a), (b), (c) shows the histograms of the distribution of drain currents (I_{dss}), pinch-off voltages (V_{po}), and gate/source breakdown voltages, respectively.

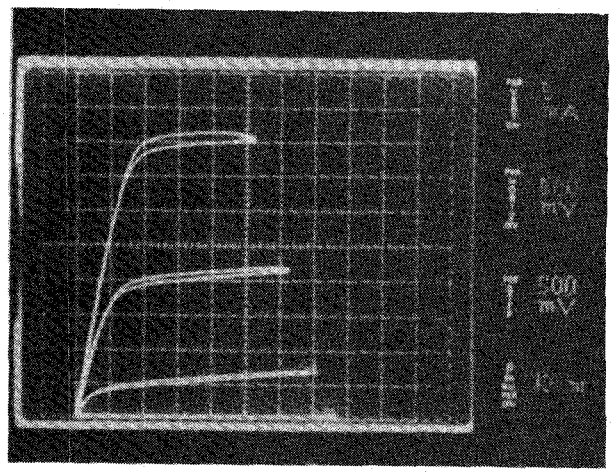

Fig. 4. Typical $I-V$ characteristics of an ion-implanted 0.5-μm-gate low-noise GaAs FET ($W_g = 300$ μm), showing high transconductance near pinch-off and low output conductance.

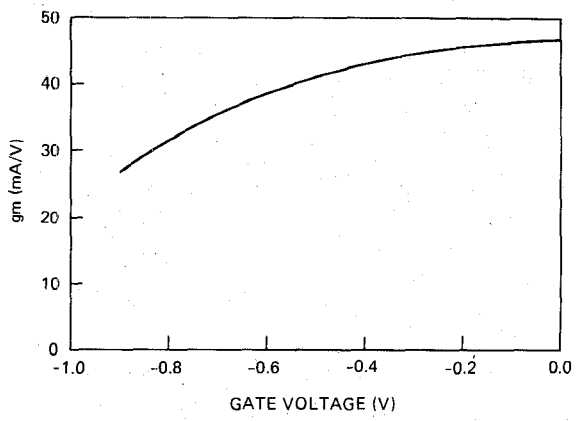

Fig. 5. Transconductance (g_m) versus gate voltage of a 0.5 μm×300 μm FET showing high g_m near pinch-off.

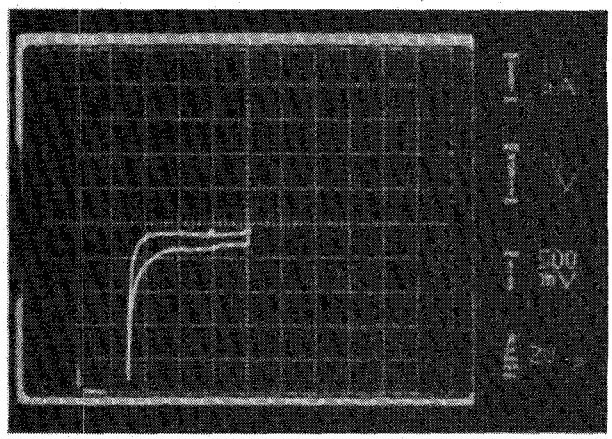

Fig. 6. Gate-to-source breakdown voltage of the 0.5-μm low-noise FET.

RF testing at 12 and 18 GHz has been conducted on the 0.5-μm-gate low-noise FET's. At 12 GHz, the average noise figure is 1.4 dB with 9.0 dB associated gain, while the best device measures 1.2 dB noise figure with 8.8 dB associated gain and 14.2 dB maximum available gain, as shown in Fig. 8. Fig. 7(d) shows the histogram of the distribution of noise figures measured at 12 GHz. At 18

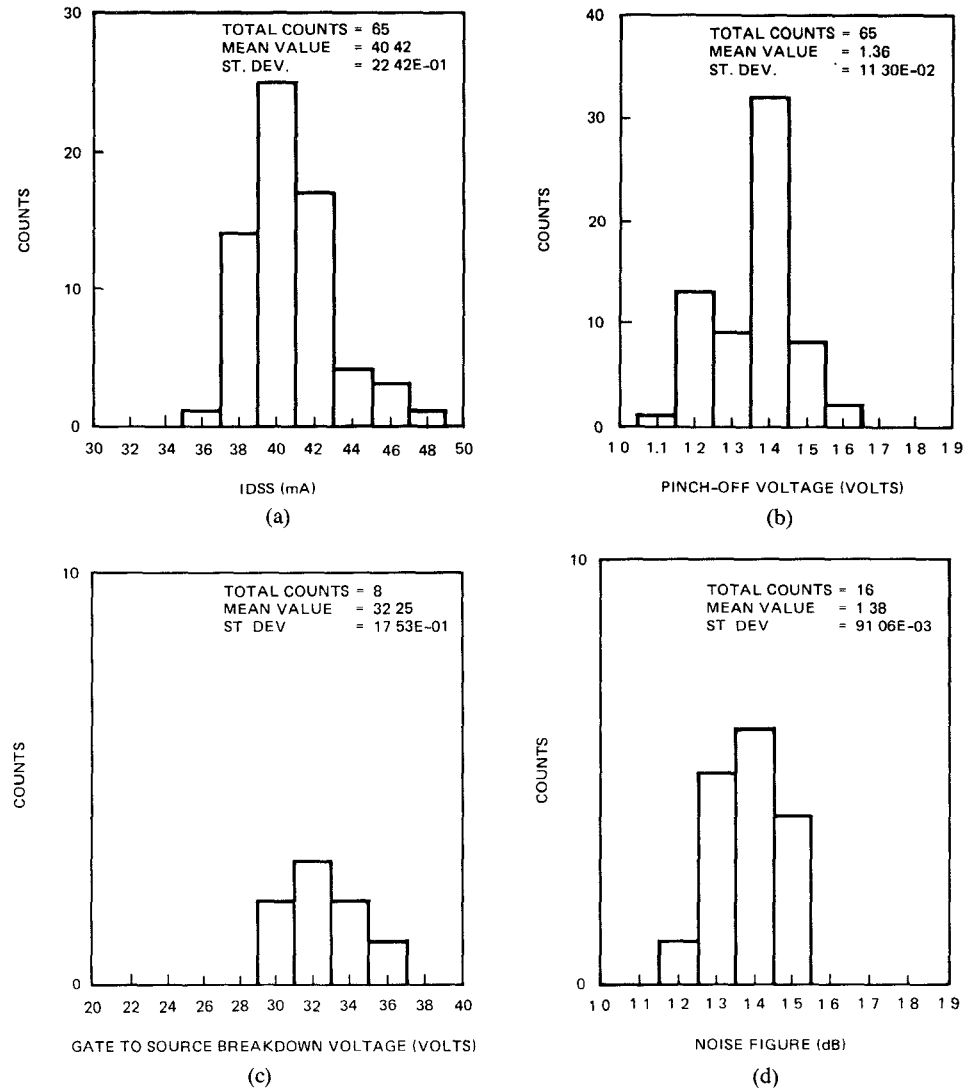

Fig 7. Histograms of the distribution of (a) drain saturation currents (I_{dss}), (b) pinch-off voltages (V_{po}) (c) gate-to-source breakdown voltages, and (d) noise figures at 12 GHz, for 0.5×300 μm FET's.

GHz, the best device shows a 1.7 dB noise figure with 6.6 dB associated gain. For comparison, results from a low-noise FET fabricated on VPE material are also included in Fig. 8. Notice that the minimum noise figure of the implanted FET is measured at a very low channel current, indicating that the device maintains high-quality channel characteristics (high transconductance, etc.) near the channel–substrate interface. In this case, better channel quality enables the implanted device to operate at lower current of 6 mA at minimum noise point, as compared to 14 mA for the VPE counterpart.

The input resistances are deduced from S-parameter measurements. The total input resistance $R_T = (R_g + R_i + R_s)$ improved from 6.9 Ω (60 keV work in [21]) or 5.9 Ω (100 keV work in [21]) to 3.4 Ω in this work, where R_g is the gate resistance, R_i is the channel charging resistance, and R_s is the source resistance. This low R_T contributes to the low-noise figure and the high maximum available gain of 14.2 dB at 12 GHz. The calculated FET noise K_f factor for the best device at 12 GHz is 1.7, which is the best reported number for an ion-implanted MESFET.

More recently, a 0.25×60 μm FET using this same channel process has been fabricated. The preliminary RF performance is very encouraging: 1.7 dB noise figure with 6.3 dB associated gain and 2.5 dB noise figure with 5.0 dB associated gain were measured at 22 GHz and 35 GHz, respectively. Table II summarizes the best noise performance of the newly developed ion-implanted FET's from X- to Ka-band.

V. Monolithic Low-Noise Amplifiers Performance

The main objective of this work is to develop a high-performance, production-adaptable FET process for MMIC applications. As a test vehicle, a 0.5-μm-gate X-band two-stage low-noise monolithic amplifier [2], [3], as shown in Fig. 9, has been fabricated using this new FET process.

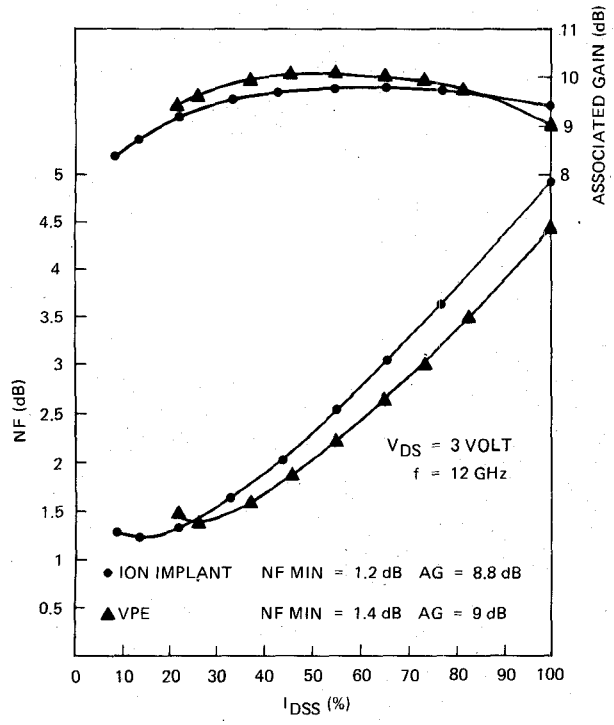

Fig. 8. Noise/gain performance of a 0.5-μm-gate ion-implanted FET at 12 GHz. Results from a VPE FET are included for comparison. The implanted FET shows a steeper doping profile, which is indicated by a lower bias current at minimum noise figure point.

TABLE II
SUMMARY OF THE BEST PERFORMANCE OF THE NEWLY DEVELOPED ION-IMPLANTED FET'S

F (GHz)	NF (dB)	AG (dB)
*12	1.2	8.8
*18	1.7	6.6
**22	1.7	6.3
**35	2.5	5.0

*0.5×300 μm FET.
**0.25×60 μm FET.

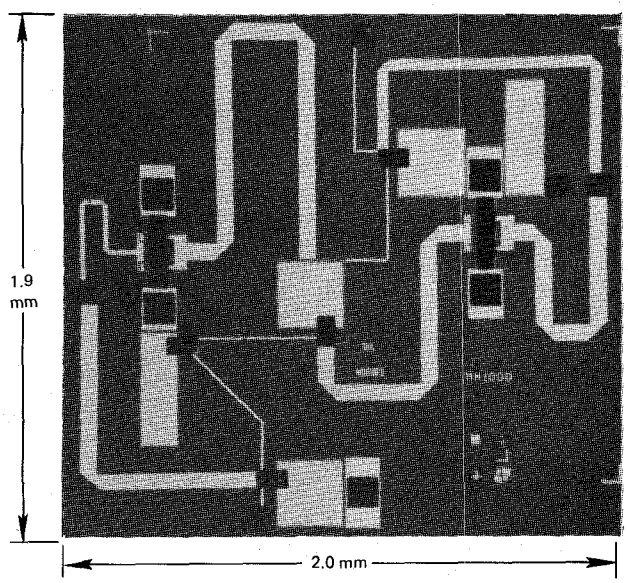

Fig. 9. Photograph of the X-band two-stage monolithic low-noise amplifier. Chip dimensions are 1.9×2.0×0.1 mm.

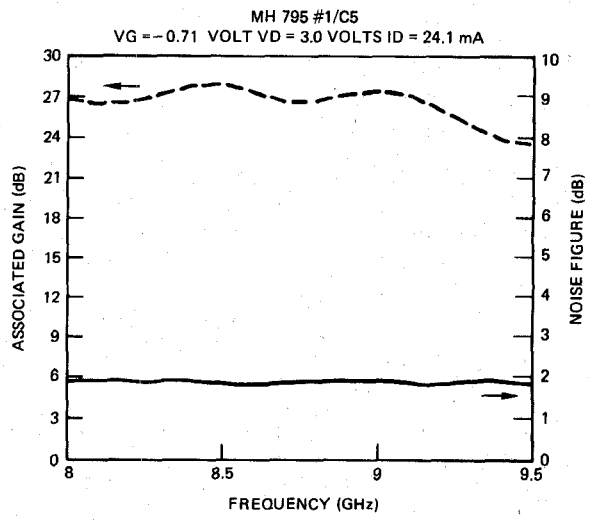

Fig. 10. Noise figure and associated gain versus frequency from a two-stage monolithic low-noise amplifier.

Additional process steps for the monolithic circuit include 2300-Å sputtered SiO_2 in the MOM capacitors, plated air bridges for low-resistive, low-capacitive connections of FET source electrodes, and via holes for low-inductive grounding. The final thickness of the amplifier chip is 4 mils.

The dc yield of the amplifier chips is 42 percent. The noise figure and associated gain of the amplifier from 8 to 9.5 GHz are plotted in Fig. 10. The gain roll-off beyond 9 GHz is the result of nonoptimized matching circuits. Nonetheless, the 1.8 dB noise figure and 23.6 dB associated gain at 9.5 GHz match the best performance from an X-band monolithic low-noise amplifier [11]. Optimized matching circuits based on the new FET model would promise to further improve the amplifier performance.

VI. SUMMARY

State-of-the-art GaAs low-noise MESFET's have been developed using a production-adaptable ion-implantation process. A 0.5-μm-gate FET has achieved a 1.2 dB noise figure with 8.8 dB associated gain at 12 GHz and a 1.7 dB noise figure with 6.6 dB associated gain at 18 GHz. More recently, a 0.25×60 μm FET has also demonstrated 1.7 dB and 2.5 dB noise figures with 6.3 dB and 5.0 dB associated gains at 22 GHz and 35 GHz, respectively. These excellent device results are attributed to the high doping density in a shallow, abrupt channel layer, coupled with selective N^+ implants in the source/drain region and a planar isolation process.

The monolithic amplifier using this FET process has demonstrated 1.8 dB noise figure with 23.6 dB associated gain at 9.5 GHz. The dc yields for the FET and amplifier chips are 47 percent and 42 percent, respectively. These results clearly demonstrate that with proper design and process, direct ion implantation is capable of producing low-cost and high-performance GaAs low-noise MESFET's for MMIC production.

ACKNOWLEDGMENT

The authors would like to thank H. Yamasaki, J. M. Schellenberg, and H. J. Kuno for their support of this work. They would also like to acknowledge the contributions of M. Siracusa, M. Mababa, A. Gomez, C. D. Chang, S. Buttles, R. Rush, H. Kanber, W. Klatskin, and D. Sensiper.

REFERENCES

[1] S. K. Wang, K. G. Wang, and C. D. Chang "High performance monolithic power amplifier using a unique ion implantation process," in *Proc. IEEE 1986 Microwave and Millimeter-Wave Monolithic Circuits Symp.*, June 1986, p. 5.

[2] S. K. Wang *et al.*, "Production technology for high-yield, high-performance GaAs monolithic amplifiers," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 2766–2771, Dec. 1985.

[3] D. C. Wang, R. G. Pauley, S. K. Wang, and L. C. T. Liu, "Cost effective high performance monolithic *X*-band low noise amplifiers," in *Proc. IEEE 1986 Microwave and Millimeter-Wave Monolithic Circuits Symp.*, June 1986, p. 61.

[4] H. Goronkin and V. Nair, "Comparison of GaAs MESFET noise figures," *IEEE Electron Device Lett.*, vol. EDL-6, p. 47, Jan. 1985.

[5] A. Higashisaka, K. Ohata, and K. Honjo, "Development of microwave GaAs MESFETs for low noise and high power applications," *Japan Tech. Rev.*, p. 145, 1982.

[6] P. C. Chao *et al.*, "Electron-beam fabrication of GaAs low-noise MESFETs using a new trilayer resist technique," *IEEE Trans. Electron Devices*, vol. EDL-32, p. 1042, June 1985.

[7] K. Kamaei *et al.*, "Quarter micron gate low noise GaAs FETs operable to 30 GHz," in *IEDM*, 1980, p. 102.

[8] H. Ishiuchi, H. Mizuno, Y. Kaneko, K. Arai, and K. Suzuki, "0.3 μm gate length super low noise GaAs MESFET," in *IEDM*, 1982, p. 590.

[9] M. Feng *et al.*, "High performance ion-implanted low noise GaAs MESFET's," *IEEE Electron Device Lett.*, vol. EDL-3, p. 327, Nov. 1982.

[10] M. Feng, V. K. Eu, T. Zielinski, H. Kanber, and W. B. Henderson, "GaAs MESFETs made by ion implantation into MOCVD buffers layers," *IEEE Electron Device Lett.*, vol. EDL-5, p. 18, Jan. 1984.

[11] R. E. Lehman and D. D. Heston, "*X*-band monolithic series feedback LNA," in *Proc. IEEE 1985 Microwave and Millimeter-Wave Monolithic Circuits Symp.*, June 1985, p. 54.

[12] H. Statz *et al.*, "Noise characteristics of gallium arsenide field-effect transistors," *IEEE Trans. Electron Devices*, vol. ED-21, p. 549, Sept. 1974.

[13] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of gallium arsenide microwave field-effect transistors, in *Advances in Electronics and Electron Physics*, vol. 38. New York: Academic Press, 1975, pp. 195–265.

[14] R. A. Pucel *et al.*, "Noise performance of gallium arsenide field effect transistors," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 243–255, Apr. 1976.

[15] W. Baechtold, "Noise behavior of GaAs field-effect transistors with short gate lengths," *IEEE Trans. Electron Devices*, vol. ED-19, p. 674, May 1972.

[16] Cappy *et al.*, "A new method for calculating the noise parameters of MESFET's and TEGFET's," *IEEE Electron Device Lett.*, vol. EDL-6, p. 270, June 1985.

[17] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-26, p. 132, 1979.

[18] H. Daembkes *et al.*, "Improved short-channel GaAs MESFET's by use of higher doping concentration," *IEEE Trans. Electron Devices*, vol. ED-31, p. 1032, Aug. 1984.

[19] F. Hasegawa, "Low Noise GaAs FETs," in *GaAs Principles and Technology*. Norwood, MA: Artech House, 1982, p. 177.

[20] Deng Xin-can "A 12 GHz planar low noise GaAs MESFET," in *Proc. 8th Biennial Cornell Conf.*, vol. 8, 1981, p. 233.

[21] M. Feng, V. K. Eu, and H. Kanber, "Optimization of ion-implanted low noise GaAs metal-semiconductor field effect transistors," *J. Appl. Phys.*, vol. 56, p. 1171, Aug. 1984.

✠

Kems-Gwor (Kenneth) Wang (M'79) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, Republic of China, in 1977 and the M.S. degree in electrical and computer engineering from the University of California at Santa Barbara (UCSB) in 1981.

While at UCSB, he worked as a graduate research assistant in the field of surface-acoustic-wave bandpass filter simulation under Dr. G. L. Matthaei. In April 1981, he joined Motorola Inc., Phoenix, AZ, where he worked as a device engineer involved in the processing and device characterization of Si microwave low-noise and UHF power n-p-n transistors, the TMOS temperature effect, GaAs tuning diodes, and GaAs dual-gate and deep-recess low-noise MESFET's. In January 1985, Mr. Wang joined the Torrance Research Center of Hughes Aircraft Company as a member of the Technical Staff, where he has been engaged in the device and process developments of *X*- and *Ku*-band high-efficiency, high-breakdown power FET's, *X*- to *V*-band low-noise MESFET's and MOCVD/MBE HEMT's, power and pseudomorphic HEMT's, AlGaAs insulated gate MISFET's, and I^2 FET's with P- buried layer. He has also been responsible for the fabrication of EW 6–18 GHz broad-band low-noise and power MMIC's, *X*-bandpush-pull high-efficiency power MMIC's, and the optimization of *X*-band two-stage power and low-noise MMIC's for production. He is currently a Device Processing Supervisor.

Mr. Wang has published more than nine technical papers in the areas of GaAs FET's, HEMT's and MMIC processing. He is also the author of a Chinese electronics book. Mr. Wang is a member of the IEEE Electron Devices Society.

✠

Shing-kuo Wang (M'76) was born in China on September 25, 1945. He received the B.S. degree in physics from National Taiwan University in 1966, and the M.S. degree in physics and the Ph.D. degree in solid-state physics from Carnegie Mellon University in 1969 and 1973, respectively.

He joined the Hughes Aircraft Company in 1983, where he is now manager of the Device and Material Technology Department in the Microwave Products Division, responsible for the development of GaAs FET devices and MMIC fabrication technology. Prior to joining Hughes, Dr. Wang was a Senior Engineer at the Westinghouse Research Center in Pittsburgh, PA. There he was involved with GaAs material processing, FET development, and MMIC fabrication technology.